TITLE

METHOD FOR CONTROLLING THE TOP WIDTH OF A TRENCH

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for fabricating a deep trench capacitor, and more particularly, to a method for controlling the upper width of a trench.

Description of the Related Art

A DRAM cell comprises a transistor and a capacitor. In order to shrink memory cell size, reduce power consumption and increase speed, the 3D capacitor of the DRAM cell is formed in the semiconductor as the deep trench capacitor combined with a transistor.

Fig. 1A is a plan view showing the deep trench capacitor of a DRAM. Each active area of the folded bit line structure comprises two word lines (WL1 and WL2) and one bit line and DT indicates the deep trench and CB indicated the bit line contact plug.

Fig. 1B is a cross-section of the deep trench capacitor of the DRAM. The deep trench (DT) is formed in the semiconductor substrate 10 and a trench capacitor 12 is formed at the bottom of the deep trench which comprising a buried plate, a node dielectric and a storage node.

The process steps of the deep trench capacitor 12 are described as follows : The deep trench (DT) is formed in the p-type semiconductor substrate 10 by reactive ion etching (RIE). N-type ions are diffused into the bottom of the deep trench DT to form a n-type diffusion area 14 used as the buried plate by diffusing heavily doped materials such as ASG with the rapid thermal

method(RTP). Thereafter, a silicon nitride layer 16 is formed on the sidewall and bottom of the deep trench (DT) used as the node dielectric of the deep trench capacitor. A first poly silicon layer 18 is deposited in the deep trench and then etched back to a target depth, which is used as the storage node of the deep trench capacitor 12.

The collar dielectric layer 20 is formed on the upper sidewall of the deep trench (DT) . The n-type doped second poly silicon layer and the third poly silicon layer 24 are formed thereafter. Furthe, the shallow trench isolation(STI)26 , the word lines(WL1 and WL2), the source/ drain 28 , the bit lines(BL)and the bit line contact plug(CB)are formed, which in the shallow trench isolation 26 is used to isolate two close DRAM cells.

In order to connect the deep trench capacitor 12 and the transistor, the buried strap out-diffusion area 30 referred to as node junction is formed on the top sidewall of the deep trench (DT). The node junction is formed by out-diffusing n-type ions in the second poly silicon layer 22 through the third poly silicon layer 24, which is called buried strap 24 into the close silicon substrate 10. The collar dielectric layer 20 effectively isolates the buried strap out diffusion area 30 and the buried strap 14 to avoid leakage and increase retention time, however, the upper width of the deep trench is enlarged during the conventional process step forming the collar dielectric layer 20, changing the distribution of the buried strap out diffusion region 30 and the overlap of the active area (AA) and the deep trench(DT). More particularly, the overlap (L) between source/drain region 28 and buried strap out diffusion region 30 is shortened, such that the leakage current through the buried

strap out-diffusion region is enlarged and the sub-Vt is decreased.

Figs 2A to Fig 2E are cross section showing the process steps of forming the conventional collar dielectric layer. As shown in Fig. 2A, the p-type semiconductor substrate 10 with the deep trench capacitor comprises a silicon nitride pad layer 32, a deep trench (DT), an n-type diffusion area 14 , a silicon nitride layer 16 and an n-type ions doped first poly silicon layer 18 . As shown in Fig. 2B, after removing the silicon nitride layer over the deep trench (DT) and etching back the first silicon layer 18, the first silicon oxide layer 34 is formed on the exposed surface of the deep trench (DT) by the thermal process to cover the upper surface of the deep trench (DT), enhancing the isolation between the n-type diffusion region 14 and the buried strap out diffusion region 30. As shown in Fig. 2C, the second silicon oxide layer 36 is formed by chemical vapor deposition (CVD) and the portion over the first poly silicon layer 18 is then removed by anisotropic etching.

As shown in Fig. 2D, the n-type ion doped second poly silicon layer 22 is deposited in the deep trench (DT) and then etched to a target depth. As shown in Fig. 2E, a portion of the first silicon oxide layer 34 and the second silicon oxide layer 36 is removed by wet etching, exposing the raised top of the second poly silicon layer 22. The recessed first silicon oxide layer 34 and the second silicon oxide layer 36 are used as the collar dielectric layer 26 of the trench capacitor, however, a portion of the silicon substrate 10 is oxidized during the process step of forming the first silicon oxide layer 34, such that the upper width of the deep trench (DT) is enlarged during the subsequent wet etching, reducing the overlap (L)

between the source/drain region 28 and the buried strap out diffusion region 30 as well as the leakage increases and sub-Vt gets lower.

The first silicon oxide layer 34 is necessary for the deep trench (DT) even though top width of the deep trench (DT) is enlarged. If the first silicon oxide layer 34 is skipped or its thickness reduced, leakage through the contact between the n-type diffusion region 14 and the buried strap out-diffusion region 30 becomes bigger. Accordingly, how to improve the collar oxide process to avoid the enlarging of the upper width of the deep trench is important.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method for controlling the top width of the trench, in which a sacrificial layer on the deep trench sidewall at the buried strap out diffusion region is formed to avoid enlarging of the upper width of the deep trench during the following process.

Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

To achieve the objects in accordance with the purpose of the invention, as embodied and broadly described herein, the invention comprises the following steps. A substrate with a trench is provided with the conductive layer formed in a portion

thereof. A sacrificial layer is formed in another portion of the trench thereon. The interval layer is removed to expose the sidewall of the trench over the conductive layer, such that the sacrificial layer and the exposed sidewall of the trench are oxidized.

Another method for controlling the top width of a trench comprises the following steps. A substrate with a trench is provided and the conductive layer is formed in a portion. A shield layer is formed in another portion of the trench. The interval layer is removed to expose the sidewall of the trench over the conductive layer, and the exposed sidewall of the trench is oxidized with the shield layer as a mask.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention.

In the figures ;

Fig. 1A is a plane view of a conventional deep trench DRAM cell.

Fig. 1B is a section view of a conventional deep trench DRAM cell.

Figs .2A-2E schematically illustrate process steps in the conventional formation of a trench structure.

Figs .3A-3J schematically illustrate process steps in the formation of a trench structure in accordance with the first embodiment of the present invention.

Fig. 3K is a section view of a deep trench DRAM cell structure in accordance with the present invention.

Figs .4A-4G schematically illustrate process steps in the formation of a trench structure in accordance with the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Aspects of present invention are now described in further detail with reference to Figs .3A-3E.

As shown in Fig. 3A, a semiconductor substrate 340 with a deep trench capacitor 342 is provided, which in the semiconductor substrate 340 may be a single crystal silicon substrate. The deep trench capacitor 342 comprises a buried plate 344, a storage dielectric layer 346 and a storage node 348, in which the buried plate 344 is used as a bottom electrode and the storage node 348 is used as the top electrode. The process steps of deep trench capacitor 342 follow. The deep trench (DT) is formed in the p-type silicon substrate 340 by reactive ion etching (RIE) with the pad layer 352 as the mask. Preferably, the depth of the trench is 5000nm~9000nm and the pad layer 352 is formed of the silicon nitride.

The n-type ions in heavily doped oxide(e.g., ASG)are diffused into the bottom of the deep trench (DT)by rapid thermal process to form a n-type diffusion region 344 used as the buried plate of the trench capacitor. The silicon nitride layer 346 is formed on the sidewall and bottom of the deep trench (DT), followed by the deposition of the n-type ion doped conductive

layer 348 in the trench (DT), in which the conducive layer may be polysilicon. The conductive layer 348 is etched back to approximately 600nm~1400nm below the surface of the substrate. Consequently, the recessed conductive layer 348 is used as the top electrode and the silicon nitride layer 346 between the n-type diffusion region 344 and the conductive layer 348 as the storage dielectric layer of the trench capacitor.

As shown in Fig. 3B, the node dielectric layer 346 over the conductive layer 348 is removed, followed by blanket deposition of the interval layer 349 in the trench and on the substrate, which in the interval layer 349 is preferably composed of TEOS. Referring to Fig. 3C, the interval layer 349a on the substrate and a portion of the interval layer 349a in the trench are removed by etching, in which the recessed top of the interval layer 349a is preferably 1200nm~1800nm below the surface of the trench. As shown in Fig. 3D, a sacrificial layer 354 is conformally deposited, preferably is deposited by CVD to form an amorphous silicon with approximate thickness 20nm~70nm. As shown in Fig. 3E, the sacrificial layer 354 is etched by anisotropic etching, for example, a reactive ion etching or a dry etching with Cl as the main etchant. Thereafter, the sacrificial layer 354, over the interval layer 349a and the substrate, is etched, such that only the sacrificial layer 354 on sidewalls of the trench over the interval layer 349a remains.

As shown in Fig. 3F, the interval layer 349a is removed by etching, for example, wet etching using HF as the main etchant. After removing interval layer 349a, the sidewall over the conductive layer in the trench is exposed. As shown in Fig. 3G, a first silicon oxide layer 351 is formed on the exposed sidewall of the trench (DT) by the thermal process to protect

the upper sidewall of the trench, enhancing the isolation between the n-type diffusion region 344 and the buried out diffusion region 362. More particularly, because the first silicon oxide layer 354a is formed on the sacrificial layer and the exposed sidewall of the trench, the top width of the deep trench is not enlarged during subsequent etching process.

As shown in Fig. 3H, a second silicon oxide layer 353 is deposited in the trench by CVD, followed by anisotropic etching to remove the second silicon oxide layer 353 over the conductive layer 348. As shown in Fig. 3I, an n-type upper conductive layer 358 is deposited in the trench and then etched back to a target depth below the surface of the substrate.

As shown in Fig. 3J, a portion of the first silicon oxide layer 351 and the second silicon oxide layer 353 over the sacrificial layer 358 are removed by wet etching to expose the raised top of the upper conductive layer. Both the first silicon oxide layer 351 and the second silicon oxide layer 353 are etched to the level of the top, such that the recessed first silicon oxide layer and the second silicon oxide layer on the upper sidewall of the trench are used as the collar dielectric layer 350 of the trench capacitor.

Fig. 3K is a cross-section showing the collar oxide process steps of the DRAM cell in accordance with the present invention. Formation of the collar dielectric layer 350 is followed by the formation of the top conductive layer 360(buried region), the buried out-diffusion region 362, the shallow trench isolation 364, word lines(WL1 and WL2), the source/drain 366, the bit line (BL), and the bit line contact plug (CB). Because these parts are not the points of the present invention, the description is not illustrated herein.

Fig. 4A~4G are sectional views showing the second embodiment in accordance with the present invention.

As shown in Fig. 4A, a semiconductor substrate 440 with a deep trench capacitor 442 is provided, which in the semiconductor substrate 440 may be a single crystal silicon substrate. The deep trench capacitor comprises a buried plate 444, a storage dielectric layer 446 and a storage node 448, in which the buried plate 448 is used as the bottom electrode and the storage node 448 is used as the top electrode. The process steps of deep trench capacitor 442 follow. The deep trench is formed in the p-type silicon substrate 440 by reactive ion etching (RIE) with the pad layer 452 as the mask. Preferably, the depth of the trench is 5000nm~9000nm and the pad layer 452 is formed of silicon nitride.

The n-type ions in heavily doped oxide (e.g., ASG) are diffused into the bottom of the deep trench (DT) by rapid thermal process to form a n-type diffusion region 444 used as the buried plate of the trench capacitor. The silicon nitride layer 446 is formed on the sidewall and bottom of the deep trench, followed by the deposition of the n-type ions doped conductive layer 448 in the trench, in which the conducive layer may be formed of polysilicon. The conductive layer 448 is etched back to approximately 600nm~1400nm below the surface of the substrate. Consequently, recessed conductive layer 448 is used as the top electrode and the silicon nitride layer 446 between the n-type diffusion region 444 and the conductive layer 448 is used as the storage dielectric layer of the trench capacitor.

As shown in Fig. 4B, the node dielectric layer over the conductive layer is removed, followed by blanket deposition of the interval layer 449 in trench and on the substrate, in which

the interval layer is preferably composed of TEOS. Referring to Fig. 4C, the interval layer 449a on the substrate and a portion of the interval layer 449ain the trench are removed by etching, in which the recessed top of the interval layer 449a is preferably 1200nm~1800nm below the surface of the trench.

As shown in Fig. 4D, a shield layer 454 is conformally deposited, preferably by CVD to form a silicon nitride layer with approximate thickness 20nm~70nm. As shown in Fig. 4E, the shield layer 454a is etched by anisotropic etching, for example, a reactive ion etching or a dry etching with Cl as the main etchant. Thereafter, the shield layer 454a over the interval layer and the substrate is etched to form the shield layer on the sidewall of the trench over the interval layer.

As shown in Fig. 4F, the interval layer 449a is removed by etching, such as wet etching using HF as the main etchant. After removing interval layer 449a, the sidewall over the conductive layer in the trench is exposed. As shown in Fig. 4G, a first silicon oxide layer 451 is formed on the exposed sidewall in the trench by thermal process to protect the upper sidewall of the trench (DT), enhancing the isolation between the n-type diffusion region 444 and the buried out diffusion region. More particularly, because the shield layer 454a avoids oxidation of the top substrate of the trench, the first silicon oxide layer 451 is only formed on the exposed surface out of the shield layer 454a.

One advantage of the present invention is that the top width of the trench is not enlarged during the follow wet etching when the sacrificial layer is formed on the top sidewall of the trench.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of thee appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.